IN THE CLAIMS:

(1) Kindly amend Claim 1 as follows:

1. (Amended) A method of manufacturing a laterally diffused metal oxide semiconductor (LDMOS) device, comprising:

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forming an amorphous region in a semiconductor substrate between isolation structures and adjacent a gate structure by implanting an amorphizing element in the semiconductor substrate; and

diffusing a channel dopant laterally in the amorphous region to form a first portion of a channel.

(2) Kindly amend Claim 6 as follows:

6. (Amended) The method as recited in Claim 1 wherein diffusing a channel dopant laterally in the amorphous region includes diffusing a first P-type source/drain dopant to a depth of about 100 nm, and implanting an amorphizing element includes implanting an amorphizing element to a depth ranging from about 180 nm to about 200 nm.

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[(3) Kindly amend Claim 7 as follows:]

7. (Amended) The method as recited in Claim 1 wherein diffusing a channel dopant laterally in the amorphous region includes diffusing a channel dopant on a first side of the gate structure and further including diffusing a source/drain dopant laterally in the semiconductor substrate and on a second side of the gate structure.

(4) Kindly amend Claim 8 as follows:

8. (Amended) The method as recited in Claim 1 wherein diffusing a channel dopant includes diffusing a channel dopant at a temperature above about 600°C that re-crystallizes the amorphous region.

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(5) Kindly amend Claim 9 as follows:

9. (Amended) The method as recited in Claim 1 wherein diffusing a channel dopant includes diffusing a channel dopant having a gaussian distribution within the amorphous region.

(6) Kindly amend Claim 11 as follows:

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11. (Amended) A method of manufacturing an integrated circuit, comprising:

fabricating laterally diffused metal oxide semiconductor (LDMOS) transistors, including:

forming an amorphous region in a semiconductor substrate between isolation structures and adjacent a gate structure by implanting an amorphizing element in the semiconductor substrate; and

diffusing a channel dopant laterally in the amorphous region to form a first portion of a channel;

depositing interlevel dielectric layers over the LDMOS transistors; and

creating interconnect structures in the interlevel dielectric layers that interconnect the LDMOS transistors to form an operative integrated circuit.

(7) Kindly amend Claim 16 as follows:

16. (Amended) The method as recited in Claim 11 wherein diffusing a channel dopant laterally in the amorphous region includes diffusing a first P-type dopant to a depth of about 100 nm, and implanting an amorphizing element includes implanting an amorphizing element to a depth ranging from about 180 nm to about 200 nm.

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(8) Kindly amend Claim 17 as follows:

17. (Amended) The method as recited in Claim 11 wherein diffusing a channel dopant laterally in the amorphous region includes diffusing a channel dopant on a first side of the gate structure and further including diffusing a source/drain dopant laterally in the semiconductor substrate and on a second side of the gate structure.

(9) Kindly amend Claim 18 as follows:

18. (Amended) The method as recited in Claim 11 wherein diffusing a channel dopant includes diffusing a channel dopant at a temperature above about 600°C that re-crystallizes the amorphous region.

(10) Kindly amend Claim 19 as follows:

19. (Amended) The method as recited in Claim 11 wherein diffusing a channel dopant includes diffusing a channel dopant having a gaussian distribution within the amorphous region.